phase of the edge of the output signal, are each a fraction of the input signal and the output signal transition times.

17. (New) A method as claimed in Claim 1 wherein the phase of the edge of the input signal is directly compared with the phase of the edge of the output signal by applying the input signal and output signal to gates of transistors which are coupled in a combinational logic circuit.

18. (New) A method as claimed in Claim 17 wherein the combinational logic circuit provides current source and drain to an output as up and down current pulses.

REMARKS

Claims 1-10 were rejected under 35 U.S.C. 102(b) as being anticipated by Saito (U.S. Patent 5,432,481). That rejection is respectfully traversed and reconsideration is requested.

The present invention is directed to a multiplier in which a phase comparator directly compares the edges of input and output signals to control the frequency of a frequency generating circuit such as a voltage controlled oscillator. As illustrated in Figs. 3 and 4, up and down pulses may be generated, for example, when fclk lags or leads dclk at their leading edges. The resultant up or down pulse is the logical combination of those signals, that combination being performed by the combinational logic circuits formed by transistors 101-103 and transistors 106-108 in figure 1. Thus, the respective signals are applied to the gates of the transistors for direct comparison. A particularly advantageous feature of the preferred embodiment is that, when the compared signals are in alignment, the up and down pulses are exceptionally short compared to those of prior art circuits. As illustrated in Figure 8, with alignment, the up pulse is only generated during the short transition time of the two clock signals. A similarly short down pulse is generated simultaneously. See column 5, line 50 through column 6, line 5 and column 6, lines 32-41.

By contrast, the Saito circuit does not directly compare the signals and does not make such a comparison in combinational circuitry. Saito does generate a window signal which, as illustrated in Figure 2B, isolates the region of the signal in which phase comparison is to be performed. As illustrated in Figure 3, that window signal output from gate G2 is applied separately to flip flops in the data path and to gate G4 in the path of the output clock 2CLK. Thus, the two signals are not directly compared but follow separate paths to the up and down voltage outputs. As illustrated in Figure 4, except through the window signal, the UP pulse width is independent of the output clock 2CLK, varying according to the phase of an edge of the data signal only. UP is dependent on DEdge, and DOWN is dependent on CEdge. It is only in the charge pump that the phases of the two signals are actually combined.

Because the two signals are not directly compared and because of the use of flip flops in the circuitry, the width of each pulse is on the order of a gate delay. By contrast, as discussed above, with the present invention the pulses can be as short as the transition time from high to low or low to high of the respective signals.

Saito does not teach every feature recited in independent claims 1 and 6. Specifically, the phase comparator of Fig. 3 does not "directly compare the phase of an edge of the input signal with the phase of an edge of the output signal." Rather, the input and output signals follow separate paths to the up and down signals.

Other aspects of the invention are further emphasized in the new dependent claims. Claims 11 and 15 recite that the phase comparator comprises combinational circuitry having an output which depends only on the state of its input. As can be seen in Figure 3 of Saito, the edge extracting and control circuits include flip flops. Thus, the comparator of Saito is of a sequential character that generates the output signal as a function of the history of the input; the output does not depend "only on the state of the input."

Claims 12 and 16 recite that the up and down pulses are each only a fraction of the transition time of the input and output signals when the signals are aligned. Even with

alignment, Saito would have up and down pulses which are substantially greater than the transition times.

Claims 17 and 18 recites that the signals gate transistors coupled in a logic gate and that those transistors drive source and drain current transistors. As noted, there is no direct comparison of the signals in Saito; there is no logic gate of transistors which receive those signals. Further, the up and down output pulses of Saito are conventional voltage pulses, not current pulses which could be applied directly to an output capacitor as in the present invention. Rather, in Saito the voltage pulses must be applied to switches SW2 and SW3 to drive the charge pump.

Claims 1-10 were rejected under the judicially created doctrine of obviousness-type double patenting in view of the parent patent 6,275,072. That rejection is overcome by the attached Terminal Disclaimer.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned at (978) 341-0036.

Respectfully submitted,

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